SYNOPSIS V1.0:

Heavy Ion Latch-up Test Results for the Maxwell SDRAM

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I. INTRODUCTION

This study was undertaken to determine the Maxwell SDRAM's susceptibility to radiation-induced latch-up, upset, functional interrupt and stuck bits. This memory was specifically packaged for SEE testing by Maxwell using Elpida/Hitachi HM5225405B die, which have been tested extensively by a variety of organizations since 1998. However, radiation performance of SDRAMs is notoriously variable. The purpose of this testing was to ensure that the performance of the JWST and SDO flight-lot SDRAMs is consistent with past results and to verify the extensive testing already undertaken by Maxwell. The data from this test are applicable to 97SD3248RPQK memories being flown by JWST, but should also apply to other 97SD and 48SD multi-chip modules from Maxwell.

The testing was done at the Texas A&M Cyclotron Facility in College Station, TX and at Brookhaven National Laboratory. The power supply current was monitored for increases, and device performance and functionality monitored with an FPGA-based controller throughout the irradiation process.

II. DEVICES TESTED

The Maxwell SDRAM single-die and stacked parts are based on a 256 Mbit 133 MHz SDRAM that was selected for its radiation performance. The device was operated with a single 3.3-volt power supply. Two samples of the device were tested.

III. TEST FACILITY

Facility: Texas A&M Cyclotron Facility.
Flux Range: $2x10^2$ to $1.3x10^5$ particles/cm^2/s.
Particles: linear energy transfer (LET)

Ion	LET (MeVcm^2/mg)
Kr	29.9
Xe	54.4

Facility: Brookhaven National Laboratory.
Flux Range: $2x10^2$ to $1.3x10^5$ particles/cm^2/s.
Particles: linear energy transfer (LET)

Ion	LET ($MeVcm^2/mg$)
C	1.45
Si	7.97
Cl	11.3
Ti	19.8

IV. TEST METHODS

Temperature: ambient temperature and 85 °C

Test Hardware: A low-speed test controller based on a Xilinx Spartan III FPGA interfaced to the DUT and a lap top computer via an RS232 protocol. (See figure 1.) The FPGA contained:

1) MicroBlaze soft core processor
2) Xilinx OPB Uart lite core (RS232 interface core)
3) Xilinx OPB Sync SDRAM controller Logicore (November 14, 2004)

The PC was a standard PC with a RS232 port. The RS232 baud rate is 115200, 8 bits, no parity, no hardware handshaking. A PC application program was used to capture the results. The data being passed from the MicroBlaze (Xilinx) was reduced (raw data). A ???? oscilloscope was used to monitor supply current for sudden rises and produced strip charts of the supply current throughout the run. Power supply current was measured every 10 ms to an accuracy of 100 pA

Software: A PC application read the RS232 port for the reduced data and added additional descriptive text. The following two types of data were sent during the test: errors and a heartbeat. The following SDRAM tests were available to be commanded via RS232 keyboard entry (using PC application program)

1) All ffffs (write once, read and verify in loop, if error found rewrite value)
2) All 0000 (same as 1)
3) All 5555 (same as 1)
4) All aaaa (same as 1)
5) Alternating 5555 and aaaa (write all values, read and verify values)

Although SELs were recorded as they occurred, the complicated errors to which SDRAMs are susceptible made it necessary to record each error for subsequent analysis to identify SEUs, SEFIs and stuck bits.

Test Techniques: Tests were performed to screen for susceptibility to latch-up, SEUs, SEFIs and stuck bits and measure sensitivity to these error modes as a function of temperature and particle LET. The ADCs were tested at room temperature, with the supply voltage, V_{cc} = 5.0 V. Equivalent normal-incidence fluences up to $1x10^7$ ions/cm^2 were used to determine the onset LET for SEL. The high LET ions used in this study precluded determination of onset LETs for SEFIs and SEUs. However, past testing has consistently shown the onset LET to be on the order of 3 MeVcm^2/mg for SEU, 10-15 MeVcm^2/mg for logic SEFIs and 35-40 MeVcm^2/mg for large SEFIs. A beam flux range of $1x10^2$ to $1.3x10^5$ particles/cm^2/s resulted in individual exposures between 10 second and 20 minutes.

Device performance and functionality were monitored with the test controller and a current-monitoring oscilloscope throughout irradiation. If the device current rose suddenly or if the device stopped functioning, we first refreshed the mode registers to see if this restored functionality. If the mode register refresh was unsuccessful, we decreased the power supply voltage incrementally to see if a holding voltage could be found before all device functionality was lost. If no holding voltage was found, we cycled power to the device and tested for functionality. Because the SDRAM is rated for a maximum power dissipation of 1 Watt, we set the limiting power supply current, I_L= 300 mA to avoid tripping the current limiting circuit due to bus contention or high current states other than SEL.

V. RESULTS

Here we summarize results of preliminary analysis of the data for SEL, SEU, SEFI and stuck bits. These results may be supplemented with additional test data after future test trips.

Single-Event Latchup

The SDRAM did not exhibit SEL up to an effective LET of 42 MeVcm^2/mg at either room temperature or at 85 °C. At 85 °C, SEL was first observed at LET= 54.4 MeVcm^2/mg for Xe, and the response was consistent with Kr incident at 60°, indicating that effective LET is at least approximately valid for SEL. At room temperature, the onset LET for SEL was between 63 MeVcm^2/mg and 73 MeVcm^2/mg. We note that these levels are somewhat lower than the corresponding levels seen during testing by Maxwell. However, they are not inconsistent with previous test results for the part, nor are they outside the variability expected for commercial memories. One difference for the current round of testing was that we irradiated the SDRAM at higher effective LET—Xe ions incident at 60°, and found that even at this high LET level, the SEL cross section did not saturate. (See figure 2.) This has two important implications:

1) It means that diffusion plays a very large role in charge collection for the SEL mechanism for these devices.
2) It suggests that standard rate calculation techniques may not reliably estimate the on-orbit rate. For this reason, we use a bounding figure-of-merit rate calculation method, yielding a rate of about 1E-4 SELs per device per day.

None of the SELs observed during this study caused prompt failure in the parts. While we cannot at present rule out the possibility that the SELs caused latent damage in the parts, there are several encouraging indications: No post-SEL functional failures have been seen in >7 years for these parts. At no time during an SEL has the supply current been seen to rise above 300 mA, which means that the power dissipation remained below the maximum rated value even

during SEL. (Note that this does not entirely eliminate the possibility of latent damage, since the dissipation of power could have been localized, leading to thermal stresses.) At present, Maxwell is waiting on the results of a post-SEL latent damage analysis from JPL that should determine with high confidence whether latent damage is a significant threat for these devices. If, as expected, the results show no indication of latent damage, this, along with the fact that the extensive testing done on these parts has yielded no indication of destructive SEL or latent damage strongly suggests that the SEL modes for these memories are nondestructive.

Single-Event Functional Interrupt

Like most SDRAMs, these parts exhibit a variety of functional interrupt modes. Often recovery from these errors was either automatic or required only a refresh of the mode registers of the device. Many errors corrupted a few hundred to a few thousand bits, although some errors resulted in very high totals of corrupted bits. The variety of error signatures exhibited by the memories made identification with software unreliable in some cases. For this reason, we opted to identify the SEFIs by hand. First we identified potential candidates as read cycles where the error rate increased by at least 3 sigma above the mean for the run. We then looked at the errors for that cycle and verified that the errors in question were consistent with a SEFI signature, rather than representing a statistical fluctuation. For the LET levels in this test, the cross section for SEFIs is effectively saturated at 1-2.0E-5 cm-2 for so-called large SEFIs and about ~1-2.0E-3 cm-2 for so-called logic SEFIs. These results are consistent with past results within a factor of 2 or so and suggest per-SDRAM-die rates on the order of once in 3 months or so for logic errors and once in about 300 years for large SEFIs. Since logic SEFIs typically affect a few words to a few hundred words, it is probable that they would be corrected by a Reed-Solomon error correction code (ECC). Some would also be corrected by a Modified Hamming code, although it should be noted that most such errors seemed to span more than a single nibble. The result of these errors if uncorrected would be several to several hundred words of corrupted data.

The large SEFIs may corrupt tens or thousands to millions of words on a single die. We note that while a Reed-Solomon type ECC would be able to correct most of these errors (except for those in words where bits were corrupted by other SEUs in other die), a Hamming Code ECC would be overwhelmed, and the data in memory would likely have to be discarded as unreliable.

In subsequent testing at Brookhaven National Laboratory, the onset LET for SEFIs was determined to be roughly 10 MeVcm^2/mg

Stuck bits

The SDRAM was tested with two refresh rates, 64 ms and 7 ms. The first 23 runs were carried out with the slower refresh rate. After about 2.7 krad(Si) of heavy-ion irradiation (heavy ions typically cause *less* damage than protons, electrons or gamma rays), we began to see errors persisting in memory after the beam had been turned off. These errors disappeared after the refresh rate was increased to 7 ms. It should be noted that stuck bits in these memories have been seen to anneal within a period of hours to days. Thus, it is unlikely that stuck bits will impact memory performance early in the mission. However, this result suggests that either not all memory cells are equally robust to TID damage or that localized damage may cause excess leakage in a single-event type process. In either case, the ability to adjust the refresh rate allows maximum throughput early in the mission and improved data integrity at end of life, when memory elements may have degraded.

Single-Event Upset

An examination of the upsets in memory during irradiation suggests that the memory is organized so that logically adjacent bits are sufficiently removed from one another that a single ion is very unlikely to result in multiple upsets in the same word. As such, most upsets would be corrected by even a Hamming Code type ECC, and are mainly a concern when they occur in conjunction with SEFIs in other die. The upset determines the desired scrub rate for the memory to avoid a high probability of ECC being overwhelmed by errors. We have done a conservative analysis and predict that the on-orbit error rate for SEU in these devices should be less than once a week per die for solar-quiet conditions. The onset LET for SEUs was determined during testing at Brookhaven National Laboratory to be roughly 1.45 MeVcm^2/mg.

Caveats

We note here that complexity of error signatures in the SDRAM precludes 100% certainty in the assignment of different individual errors to any given error mode. We have chosen to err on the side of caution, and the assignments made tend to drive the errors quoted here toward the conservative side. Having said this, the error rates quoted here are at least order-or-magnitude correct. If it is found that the rates quoted here are marginal for the application, the analysis can be revisited.

It should also be noted that the significantly higher SEL rate quoted here does not derive solely from a more conservative analysis. We also tested to significantly higher effective LET and saw that the cross section effectively did not saturate. This gives rise to a significantly higher cross section, while at the same time increasing the uncertainty for the calculation. While it is thought that the errors are more likely to drive the calculated rate toward the conservative side, it should be remembered that SEE rates for SDRAMs carry a greater uncertainty than those for other technologies. This makes the post-SEL screening results critical for this part. If no evidence of latent damage is found, these events are most likely nondestructive, and qualification of the parts is relatively easy.

VI. COMMENTS AND RECOMMENDATIONS

SDRAMs have a level of complexity in both their operation and error modes that makes them challenging for spaceflight applications. This, coupled with the fact that their SEE rates and TID performance can vary dramatically from lot to lot makes it inadvisable to fly these devices without significant mitigation of these error/failure modes. The susceptibility of these devices to SEL necessitates the incorporation of power-cycling capability in the design. At the same time, these devices have been the subject of SEE tests for over 7 years to date, and they have exhibited sufficient consistency that we have confidence that the parts will fulfill their functions provided adequate mitigation measures are implemented to ameliorate the effects of error modes.

In general, devices are categorized based on heavy ion test data into one of the four following categories:

Category 1: Recommended for usage in all NASA/GSFC spaceflight applications.
Category 2: Recommended for usage in NASA/GSFC spaceflight applications, but may require mitigation techniques.
Category 3: Recommended for usage in some NASA/GSFC spaceflight applications, but requires extensive mitigation techniques or hard failure recovery mode.
Category 4: Not recommended for usage in any NASA/GSFC spaceflight applications.
Research Test Vehicle: Please contact the P.I. before utilizing this device for spaceflight applications

The Maxwell SDRAM parts are Category 3 devices.